


GA-78LMT-S2PT

Revision :4.1

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10	RS780 SYSTEM I/F,STRAP
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19	LAN AR8161/8151
20	AUDIO ALC887 / VT1708S AUDIO JACK
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22	IT8720 LPC IO ,Dual-BIOS, KB/MS
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24	ATX, FRONT PANEL
25	VCORE (PWMISL6324+6612A)

[illegible]

				
Title				
<div>COVER SHEET</div>				
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Model Name:GA-78LMT-S2PT

Component value change history


Version: 4.1

P-Code: U11120-0

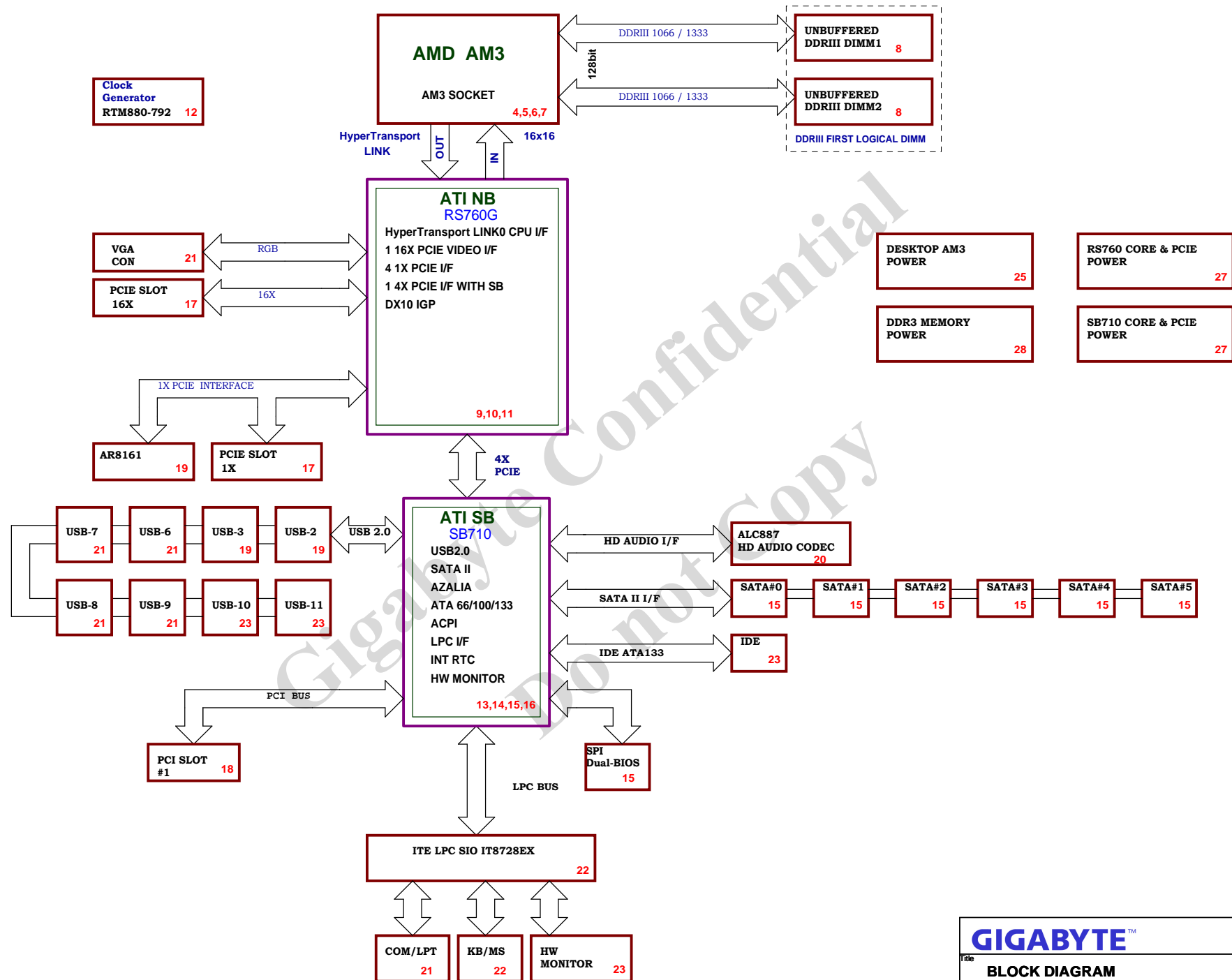
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Circuit or PCB layout change for next version

[illegible]

			
Title			
BOM & PCB HISTORY			
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RS780L CUSTOMER DESKTOP DESIGN



L0_CADIN_L[0..15] [9]
L0_CADIN_H[0..15] [9]

L0_CADOUT_L[0..15] [9]
L0_CADOUT_H[0..15] [9]

M2CPUA

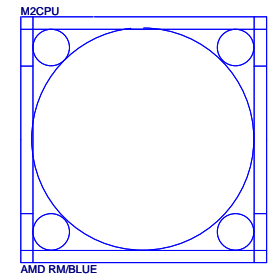
HYPERTRANSPORT

[9] L0_CLKIN_H1	L0_CLKIN_H1	N6	L0_CLKIN_H(1)	L0_CLKOUT_H(1)	AD5	L0_CLKOUT_H1	L0_CLKOUT_H1	[9]
[9] L0_CLKIN_L1	L0_CLKIN_L1	P6	L0_CLKIN_L(1)	L0_CLKOUT_L(1)	AD4	L0_CLKOUT_L1	L0_CLKOUT_L1	[9]
[9] L0_CLKIN_H0	L0_CLKIN_H0	N3	L0_CLKIN_H(0)	L0_CLKOUT_H(0)	AD1	L0_CLKOUT_H0	L0_CLKOUT_H0	[9]
[9] L0_CLKIN_L0	L0_CLKIN_L0	N2	L0_CLKIN_L(0)	L0_CLKOUT_L(0)	AC1	L0_CLKOUT_L0	L0_CLKOUT_L0	[9]
[9] L0_CTLIN_H1	L0_CTLIN_H1	V4	L0_CTLIN_H(1)	L0_CTLOUT_H(1)	Y6	L0_CTLOUT_H1	L0_CTLOUT_H1	[9]
[9] L0_CTLIN_L1	L0_CTLIN_L1	V5	L0_CTLIN_L(1)	L0_CTLOUT_L(1)	W6	L0_CTLOUT_L1	L0_CTLOUT_L1	[9]
[9] L0_CTLIN_H0	L0_CTLIN_H0	U1	L0_CTLIN_H(0)	L0_CTLOUT_H(0)	W2	L0_CTLOUT_H0	L0_CTLOUT_H0	[9]
[9] L0_CTLIN_L0	L0_CTLIN_L0	V1	L0_CTLIN_L(0)	L0_CTLOUT_L(0)	W3	L0_CTLOUT_L0	L0_CTLOUT_L0	[9]
L0_CADIN_H15	L0_CADIN_H15	U6	L0_CADIN_H(15)	L0_CADOUT_H(15)	Y5	L0_CADOUT_H15	L0_CADOUT_H15	
L0_CADIN_L15	L0_CADIN_L15	V6	L0_CADIN_L(15)	L0_CADOUT_L(15)	Y4	L0_CADOUT_L15	L0_CADOUT_L15	
L0_CADIN_H14	L0_CADIN_H14	T4	L0_CADIN_H(14)	L0_CADOUT_H(14)	AB6	L0_CADOUT_H14	L0_CADOUT_H14	
L0_CADIN_L14	L0_CADIN_L14	T5	L0_CADIN_L(14)	L0_CADOUT_L(14)	AB6	L0_CADOUT_L14	L0_CADOUT_L14	
L0_CADIN_H13	L0_CADIN_H13	R6	L0_CADIN_H(13)	L0_CADOUT_H(13)	AB5	L0_CADOUT_H13	L0_CADOUT_H13	
L0_CADIN_L13	L0_CADIN_L13	T6	L0_CADIN_L(13)	L0_CADOUT_L(13)	AB4	L0_CADOUT_L13	L0_CADOUT_L13	
L0_CADIN_H12	L0_CADIN_H12	P4	L0_CADIN_H(12)	L0_CADOUT_H(12)	AD6	L0_CADOUT_H12	L0_CADOUT_H12	
L0_CADIN_L12	L0_CADIN_L12	P5	L0_CADIN_L(12)	L0_CADOUT_L(12)	AC6	L0_CADOUT_L12	L0_CADOUT_L12	
L0_CADIN_H11	L0_CADIN_H11	M4	L0_CADIN_H(11)	L0_CADOUT_H(11)	AF6	L0_CADOUT_H11	L0_CADOUT_H11	
L0_CADIN_L11	L0_CADIN_L11	M5	L0_CADIN_L(11)	L0_CADOUT_L(11)	AE6	L0_CADOUT_L11	L0_CADOUT_L11	
L0_CADIN_H10	L0_CADIN_H10	L6	L0_CADIN_H(10)	L0_CADOUT_H(10)	AF5	L0_CADOUT_H10	L0_CADOUT_H10	
L0_CADIN_L10	L0_CADIN_L10	M6	L0_CADIN_L(10)	L0_CADOUT_L(10)	AF4	L0_CADOUT_L10	L0_CADOUT_L10	
L0_CADIN_H9	L0_CADIN_H9	K4	L0_CADIN_H(9)	L0_CADOUT_H(9)	AH6	L0_CADOUT_H9	L0_CADOUT_H9	
L0_CADIN_L9	L0_CADIN_L9	K5	L0_CADIN_L(9)	L0_CADOUT_L(9)	AG6	L0_CADOUT_L9	L0_CADOUT_L9	
L0_CADIN_H8	L0_CADIN_H8	J6	L0_CADIN_H(8)	L0_CADOUT_H(8)	AH5	L0_CADOUT_H8	L0_CADOUT_H8	
L0_CADIN_L8	L0_CADIN_L8	K6	L0_CADIN_L(8)	L0_CADOUT_L(8)	AH4	L0_CADOUT_L8	L0_CADOUT_L8	
L0_CADIN_H7	L0_CADIN_H7	U3	L0_CADIN_H(7)	L0_CADOUT_H(7)	Y1	L0_CADOUT_H7	L0_CADOUT_H7	
L0_CADIN_L7	L0_CADIN_L7	U2	L0_CADIN_L(7)	L0_CADOUT_L(7)	W1	L0_CADOUT_L7	L0_CADOUT_L7	
L0_CADIN_H6	L0_CADIN_H6	R1	L0_CADIN_H(6)	L0_CADOUT_H(6)	AA2	L0_CADOUT_H6	L0_CADOUT_H6	
L0_CADIN_L6	L0_CADIN_L6	T1	L0_CADIN_L(6)	L0_CADOUT_L(6)	AA3	L0_CADOUT_L6	L0_CADOUT_L6	
L0_CADIN_H5	L0_CADIN_H5	R3	L0_CADIN_H(5)	L0_CADOUT_H(5)	AB1	L0_CADOUT_H5	L0_CADOUT_H5	
L0_CADIN_L5	L0_CADIN_L5	R2	L0_CADIN_L(5)	L0_CADOUT_L(5)	AA1	L0_CADOUT_L5	L0_CADOUT_L5	
L0_CADIN_H4	L0_CADIN_H4	N1	L0_CADIN_H(4)	L0_CADOUT_H(4)	AC2	L0_CADOUT_H4	L0_CADOUT_H4	
L0_CADIN_L4	L0_CADIN_L4	P1	L0_CADIN_L(4)	L0_CADOUT_L(4)	AC3	L0_CADOUT_L4	L0_CADOUT_L4	
L0_CADIN_H3	L0_CADIN_H3	L1	L0_CADIN_H(3)	L0_CADOUT_H(3)	AE2	L0_CADOUT_H3	L0_CADOUT_H3	
L0_CADIN_L3	L0_CADIN_L3	M1	L0_CADIN_L(3)	L0_CADOUT_L(3)	AE3	L0_CADOUT_L3	L0_CADOUT_L3	
L0_CADIN_H2	L0_CADIN_H2	L3	L0_CADIN_H(2)	L0_CADOUT_H(2)	AF1	L0_CADOUT_H2	L0_CADOUT_H2	
L0_CADIN_L2	L0_CADIN_L2	L2	L0_CADIN_L(2)	L0_CADOUT_L(2)	AE1	L0_CADOUT_L2	L0_CADOUT_L2	
L0_CADIN_H1	L0_CADIN_H1	J1	L0_CADIN_H(1)	L0_CADOUT_H(1)	AG2	L0_CADOUT_H1	L0_CADOUT_H1	
L0_CADIN_L1	L0_CADIN_L1	K1	L0_CADIN_L(1)	L0_CADOUT_L(1)	AG3	L0_CADOUT_L1	L0_CADOUT_L1	
L0_CADIN_H0	L0_CADIN_H0	J3	L0_CADIN_H(0)	L0_CADOUT_H(0)	AH1	L0_CADOUT_H0	L0_CADOUT_H0	
L0_CADIN_L0	L0_CADIN_L0	J2	L0_CADIN_L(0)	L0_CADOUT_L(0)	AG1	L0_CADOUT_L0	L0_CADOUT_L0	

CPU-SK941AM3/S/15u[10SC1-A01942-01R_10SC1-A01942-03R]

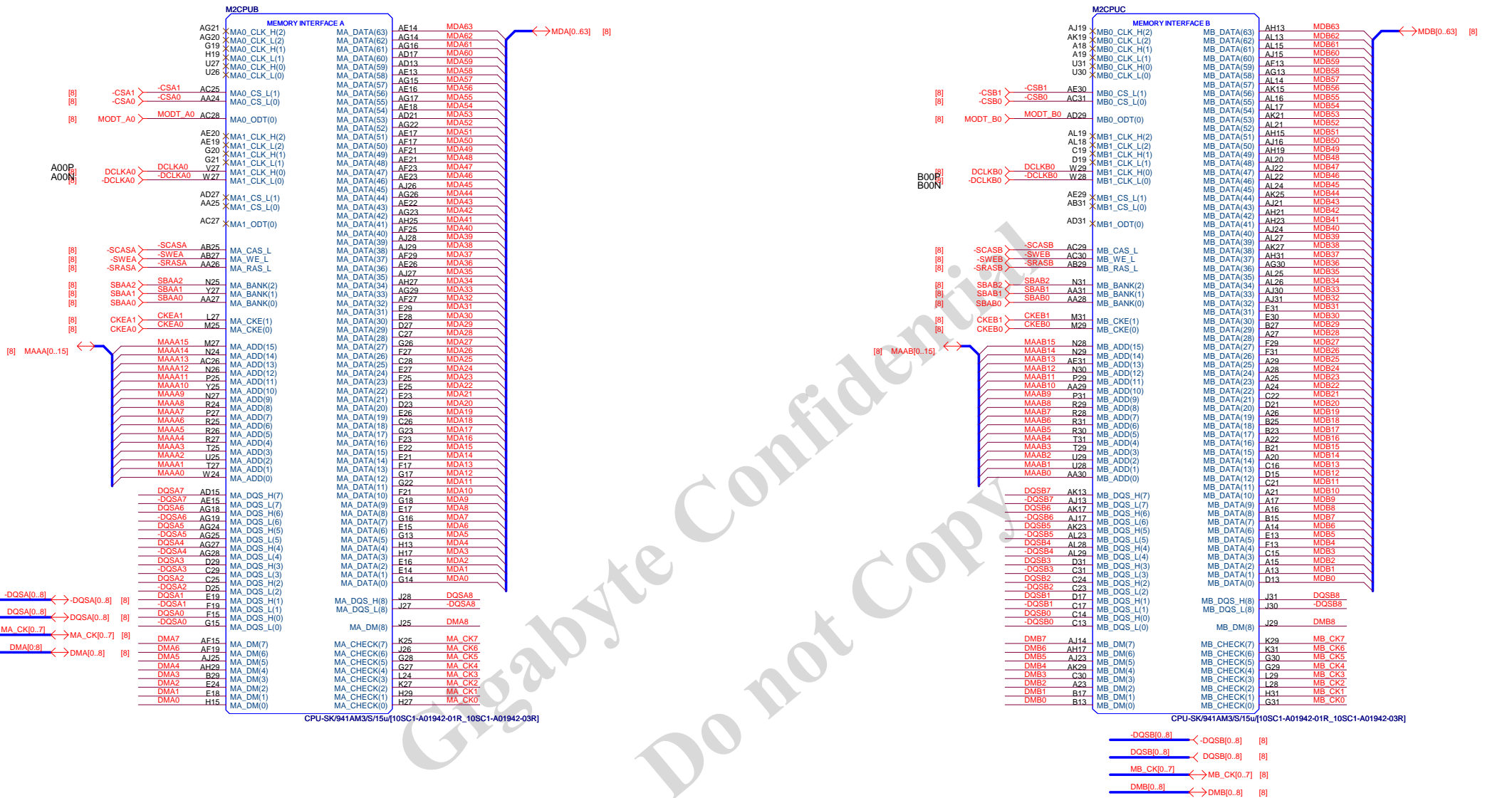
CPU_VDD_RUN = VCORE
CPU_VDDA_RUN = VDDA25
VLDT_RUN = VCC12_HT
CPU_VDDIO_SUS = DDR18V
CPU_VTT_SUS = DDRVTT

VLDT_A = VCC12_HT
VLDT_B = HT12B



AMD RM/BLUE

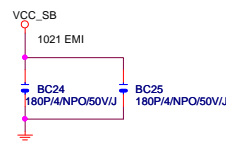
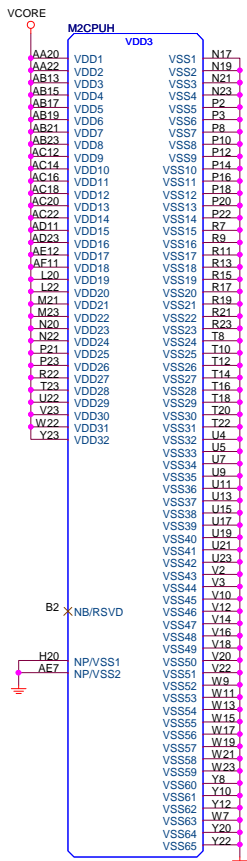
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CPU HYPER TRANSPORT			
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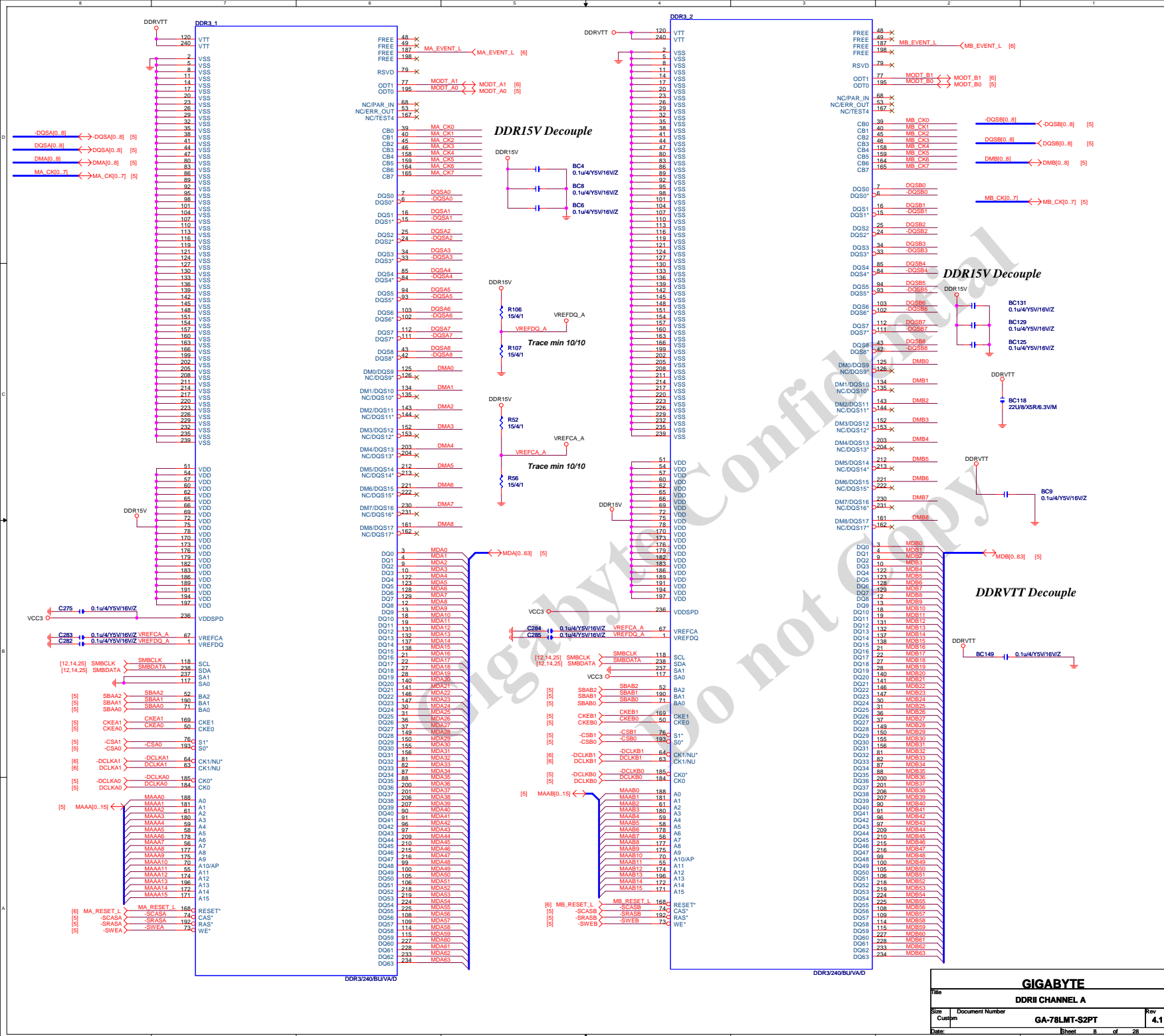


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CPU DDRII MEMORY

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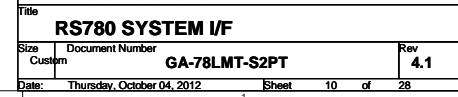
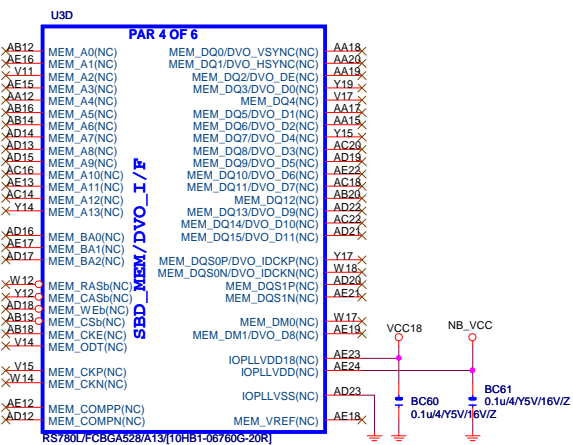


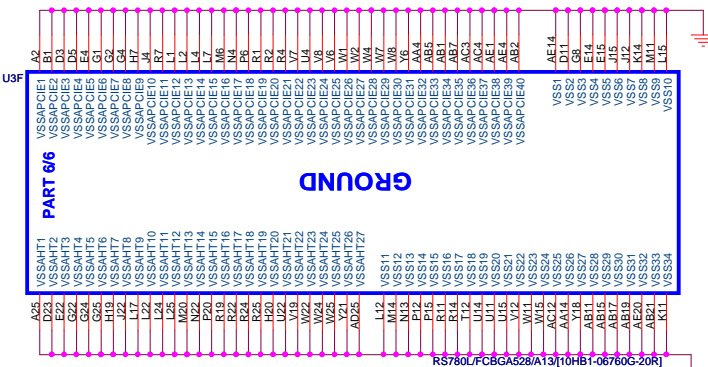
Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8

[21] DAC_VSYNC << R276 3K/4/1 VCC3

Note: for RX780, change following
pull-down resistor to 3K accordingly

[21] DAC_HSYNC << R285 3K/4/1 OVCC3

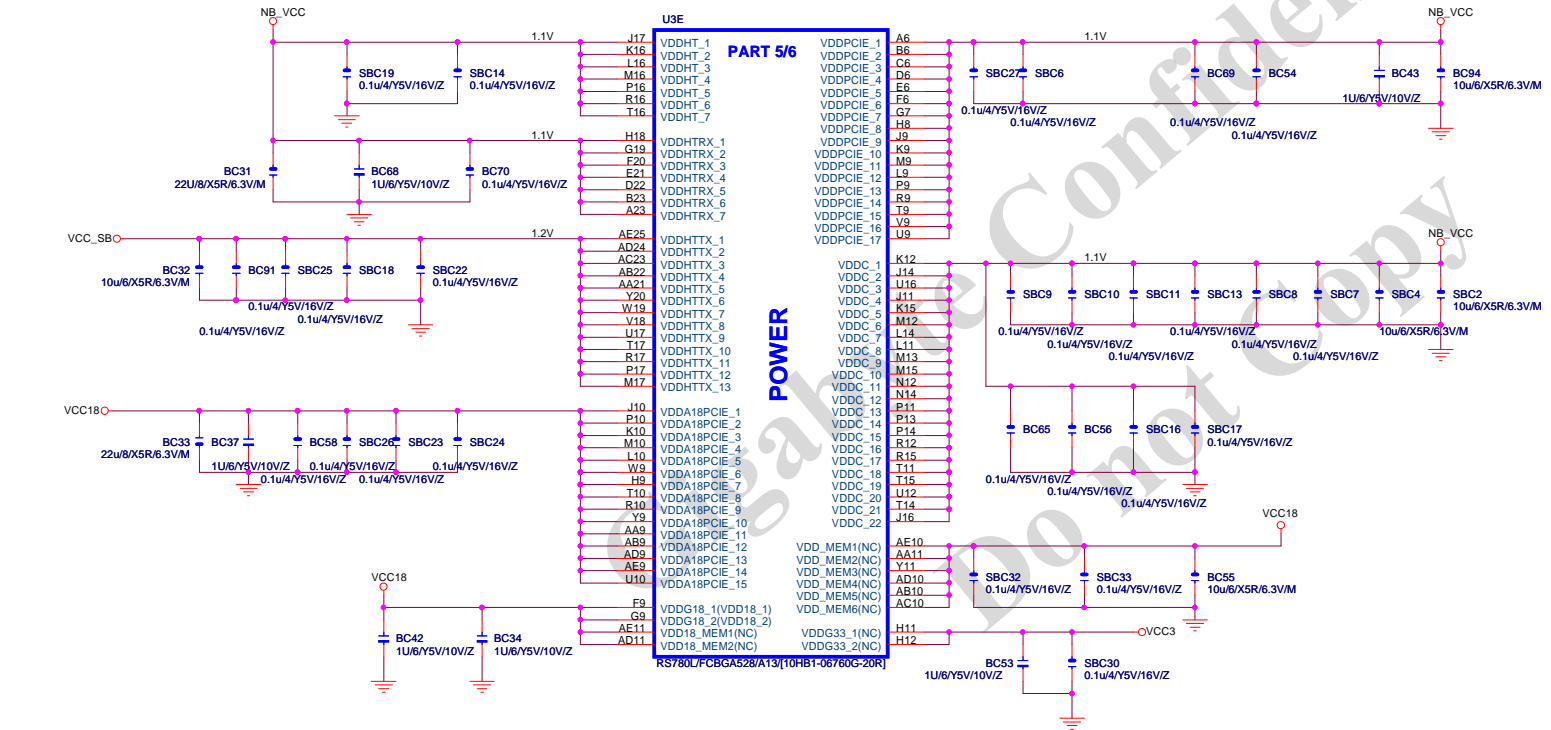


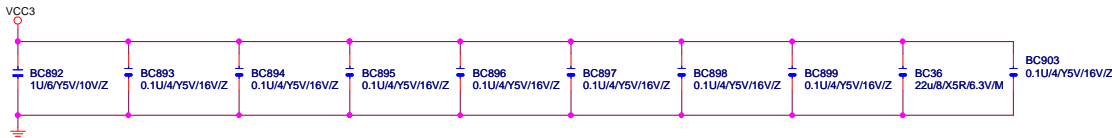


Please use 1mm pad size,
place all ELT test pads
on bottom side only

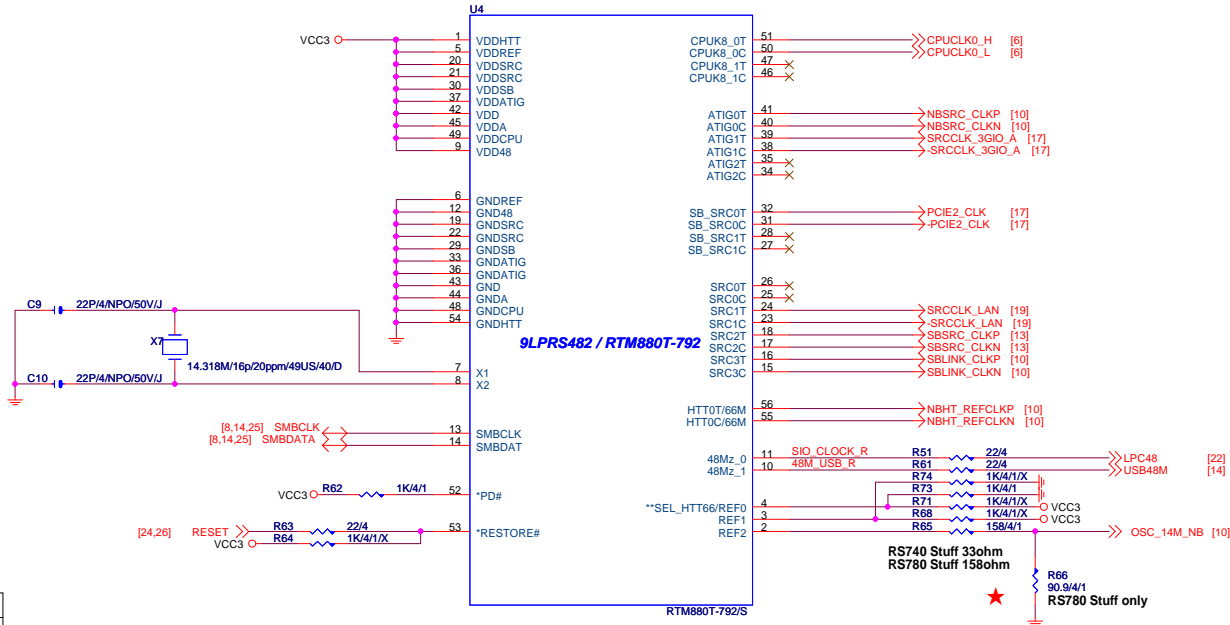
RS740/RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP18	+1.8V	NC	+1.8V





- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



watch dog --
RESTORE# 接 RESET

	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

**SEL_HTT66/REF0		OUT 3.3V 14.318MHz REF output.
IN	Low	100MHz differential HT clock, (Internal 120KΩ pull-down)
	High	66MHz 3.3V single ended HT clock.

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

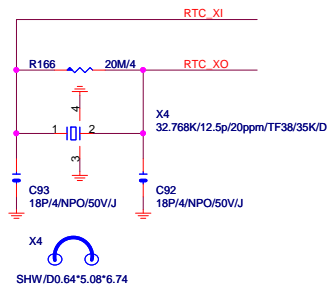
* the GFX_REFCLK input is required for all cases

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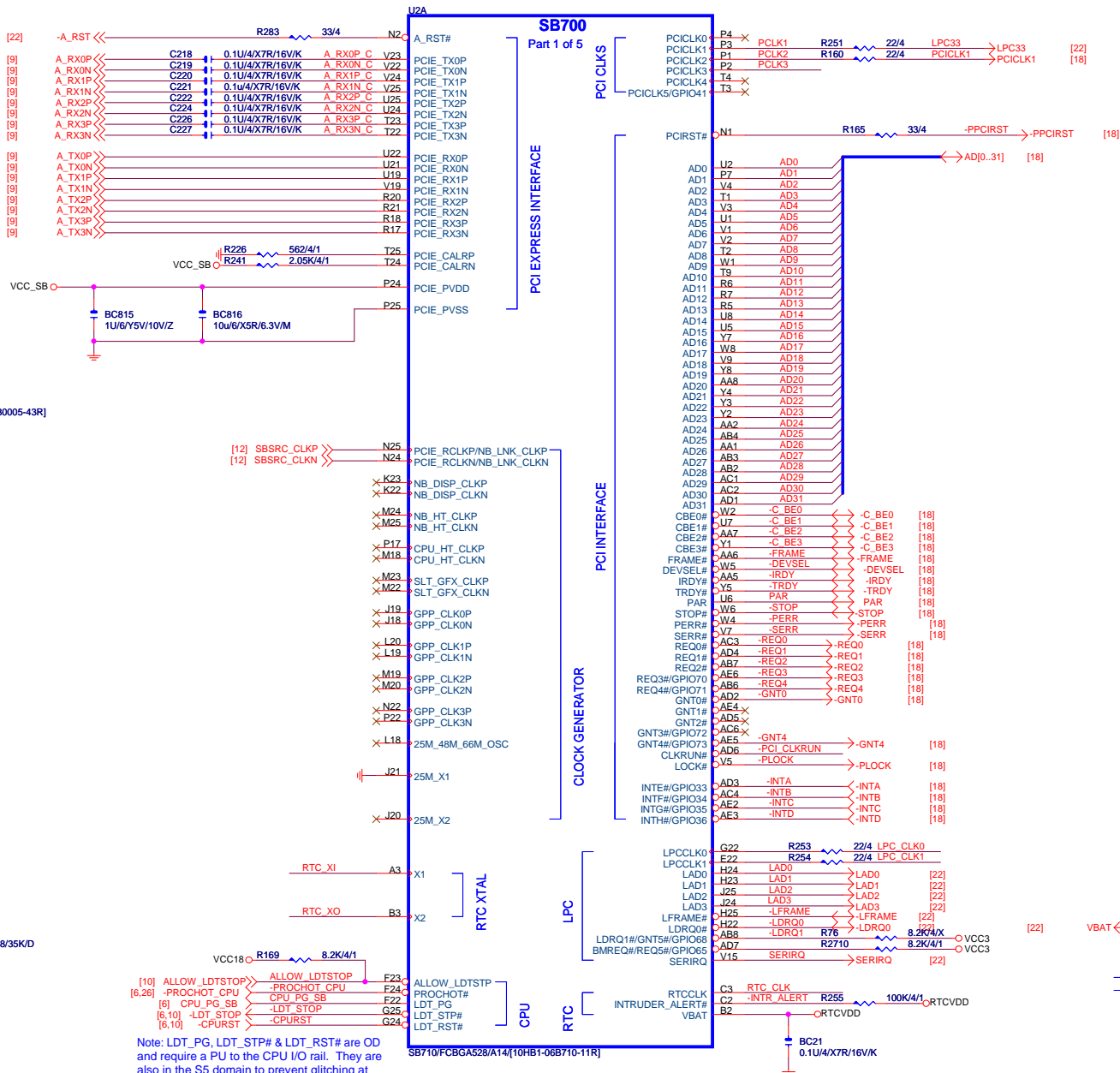
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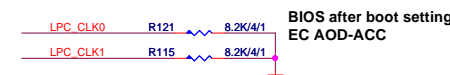
SB_HS/[12SP2-030005-41R_12SP2-030005-42R_12SP2-030005-43R]



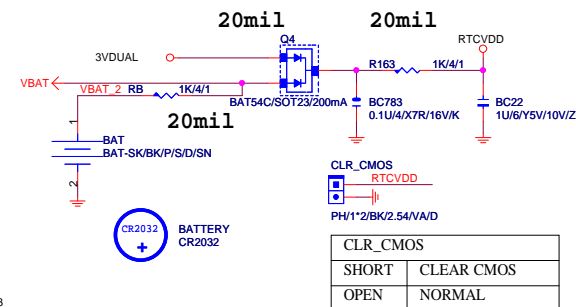
Note: LDT_PG, LDT_STP# & LDT_RST# are OD and require a PU to the CPU I/O rail. They are also in the S5 domain to prevent glitching at power up.



	PCLK2	PCLK3
PULL HIGH	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS
PULL LOW	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT



	LPC_CLK0	LPC_CLK1
PULL HIGH	IMC ENABLED	CLKGEN ENABLED
PULL LOW	IMC DISABLED AOD Extreme DEFAULT	CLKGEN DISABLED DEFAULT

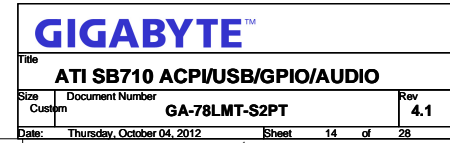


NOT ADD ICT FOR RTCVDD PIN

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Title	ATI SB710 PCIE/PC/CPU/LPC
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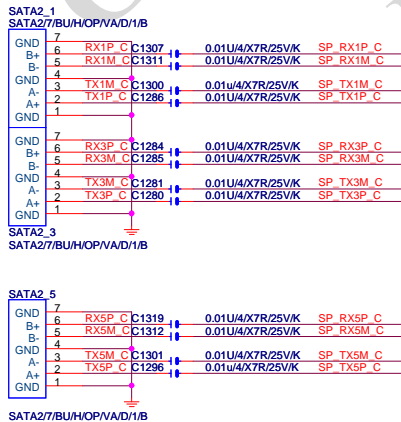
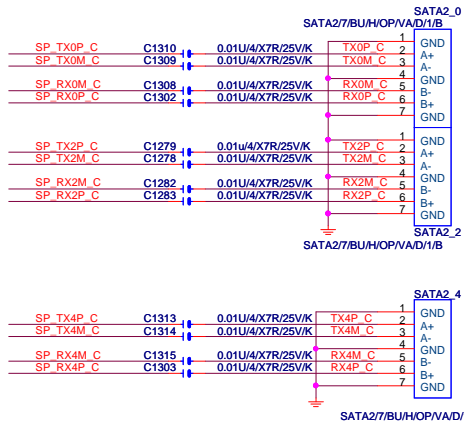
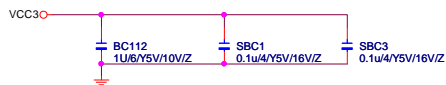
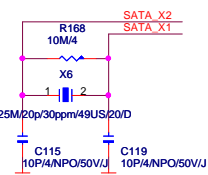
PLACE SATA AC COUPLING
CAPS CLOSE TO SB600



PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:

R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

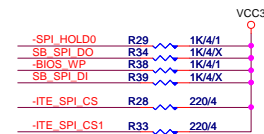
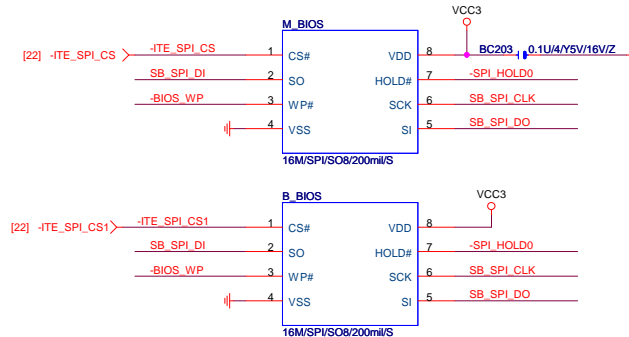
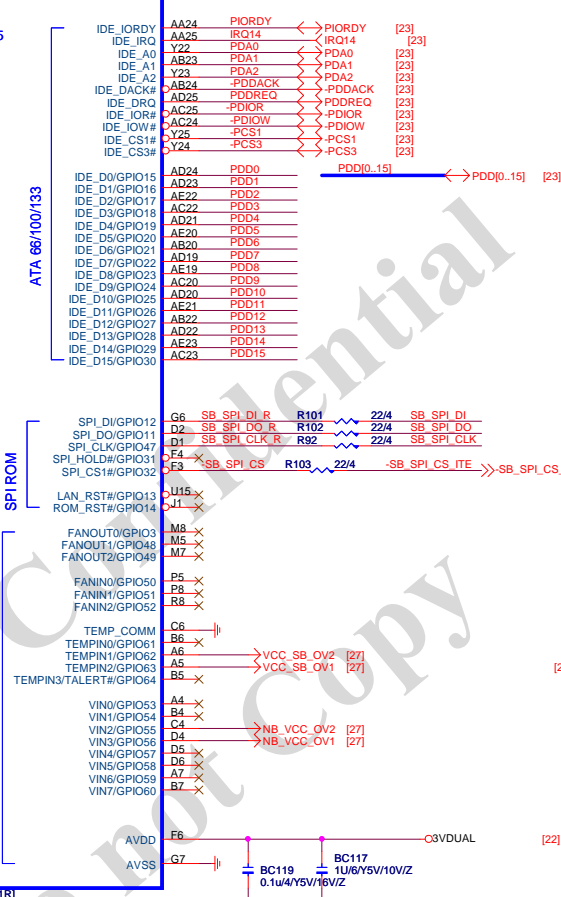


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SERIAL ATA

SATA PWR

HW MONITOR



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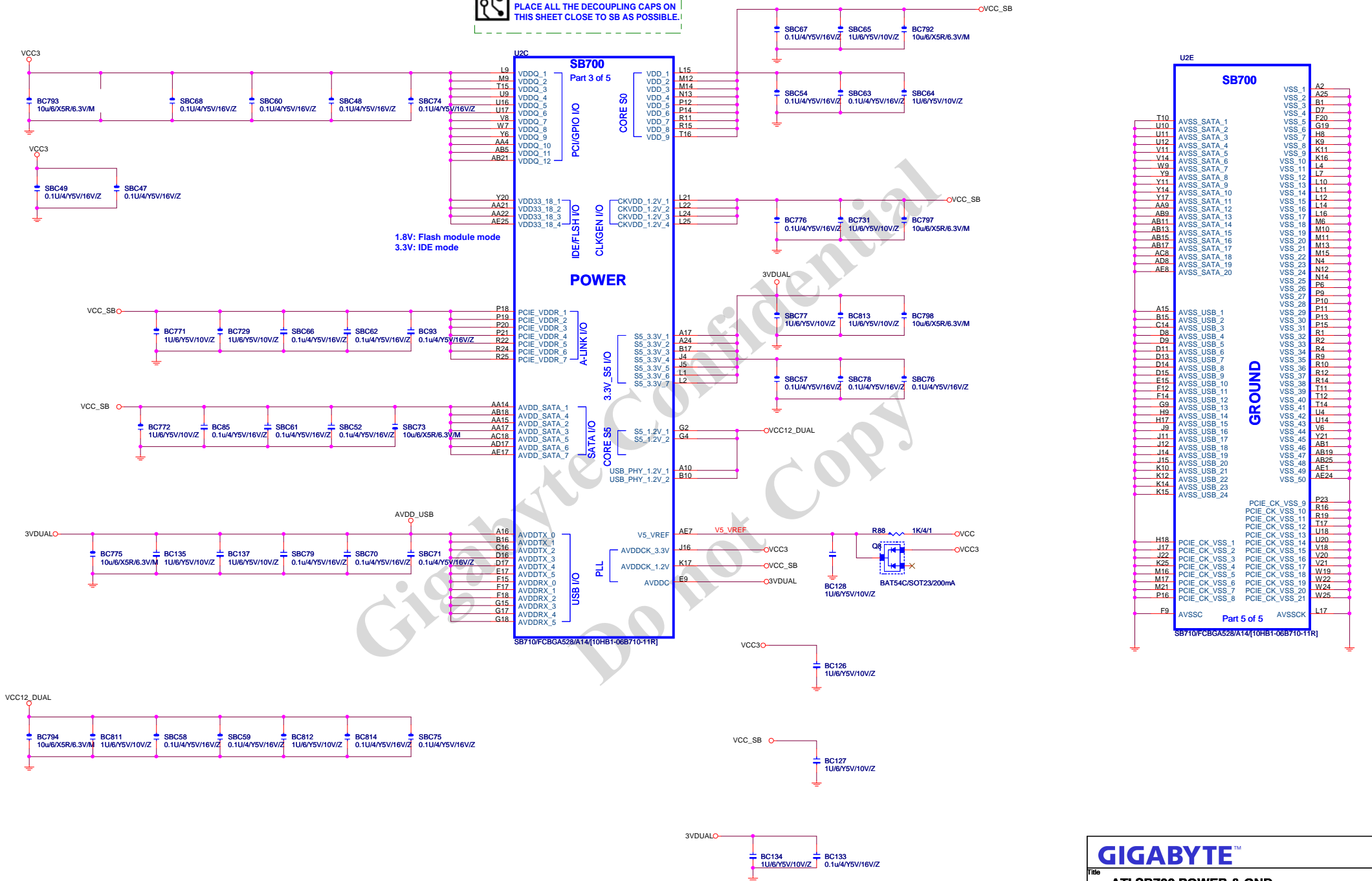
ATI SB710 SATA/IDE/HWM/SPI

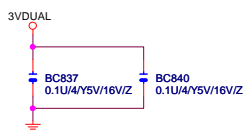
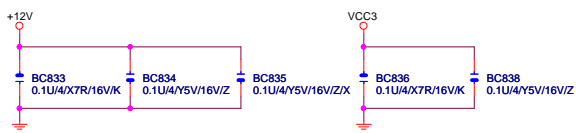
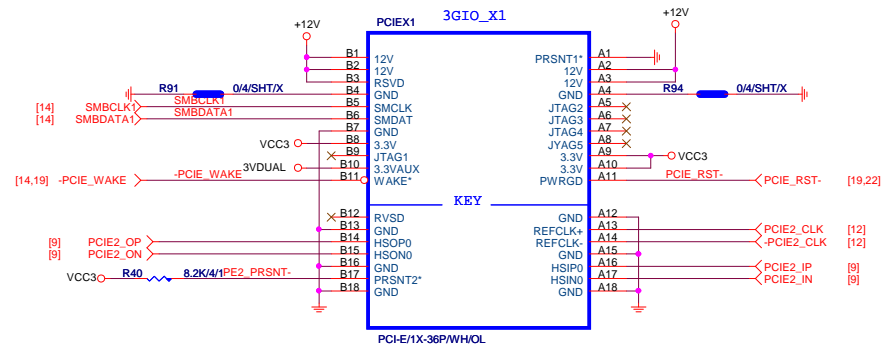
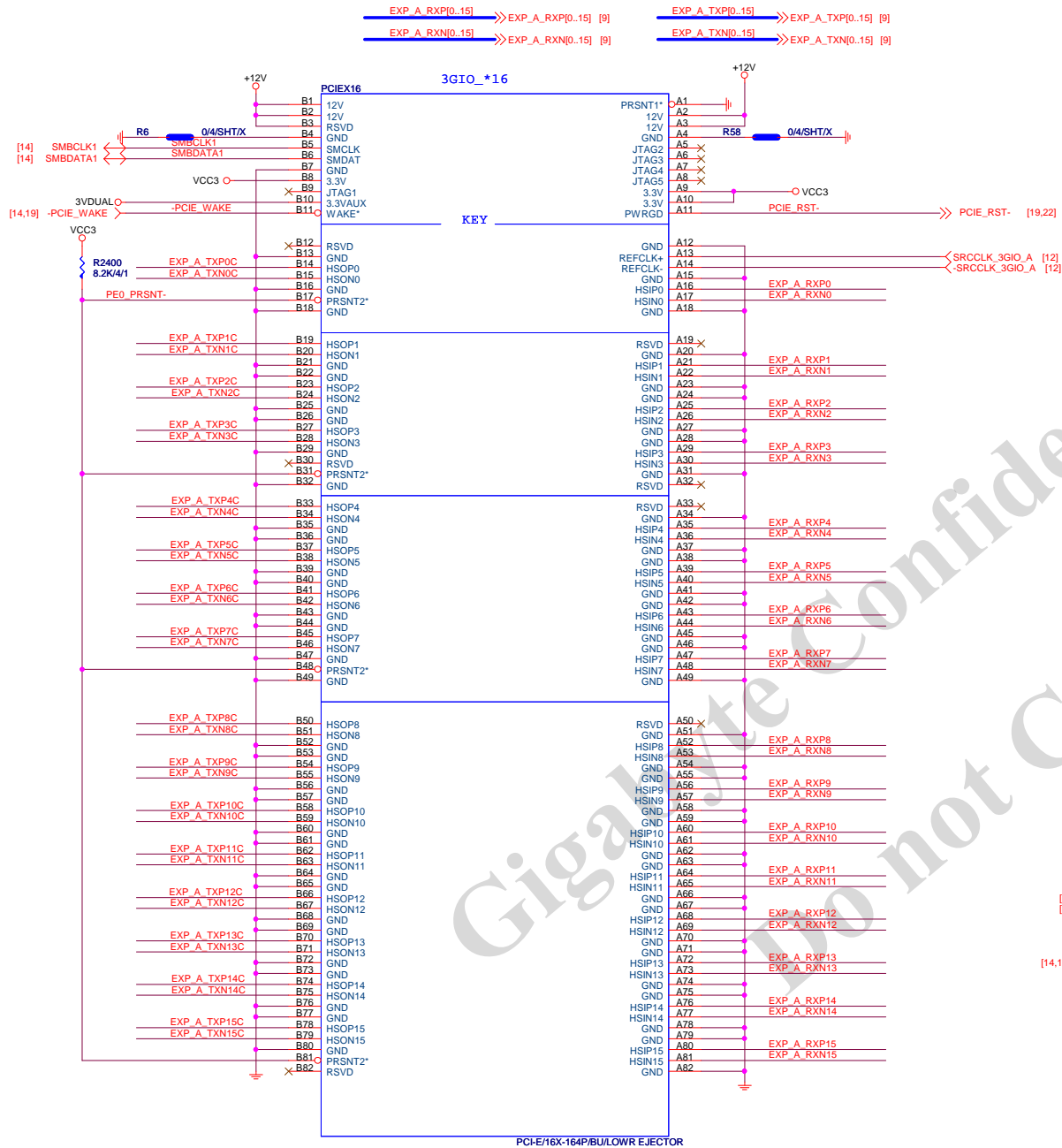
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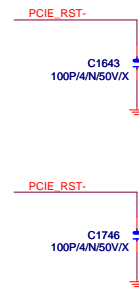


PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.





EXP A TXP0	C1644	0.1U/4X7R/16V/K	EXP A TXP0C
EXP A TXN0	C1645	0.1U/4X7R/16V/K	EXP A TXN0C
EXP A TXP1	C1646	0.1U/4X7R/16V/K	EXP A TXP1C
EXP A TXN1	C1647	0.1U/4X7R/16V/K	EXP A TXN1C
EXP A TXP2	C1648	0.1U/4X7R/16V/K	EXP A TXP2C
EXP A TXN2	C1649	0.1U/4X7R/16V/K	EXP A TXN2C
EXP A TXP3	C1650	0.1U/4X7R/16V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1U/4X7R/16V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1U/4X7R/16V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1U/4X7R/16V/K	EXP A TXN4C
EXP A TXP5	C1654	0.1U/4X7R/16V/K	EXP A TXP5C
EXP A TXN5	C1655	0.1U/4X7R/16V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1U/4X7R/16V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1U/4X7R/16V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1U/4X7R/16V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1U/4X7R/16V/K	EXP A TXN7C
EXP A TXP8	C1660	0.1U/4X7R/16V/K	EXP A TXP8C
EXP A TXN8	C1661	0.1U/4X7R/16V/K	EXP A TXN8C
EXP A TXP9	C1662	0.1U/4X7R/16V/K	EXP A TXP9C
EXP A TXN9	C1663	0.1U/4X7R/16V/K	EXP A TXN9C
EXP A TXP10	C1664	0.1U/4X7R/16V/K	EXP A TXP10C
EXP A TXN10	C1665	0.1U/4X7R/16V/K	EXP A TXN10C
EXP A TXP11	C1666	0.1U/4X7R/16V/K	EXP A TXP11C
EXP A TXN11	C1667	0.1U/4X7R/16V/K	EXP A TXN11C
EXP A TXP12	C1668	0.1U/4X7R/16V/K	EXP A TXP12C
EXP A TXN12	C1669	0.1U/4X7R/16V/K	EXP A TXN12C
EXP A TXP13	C1670	0.1U/4X7R/16V/K	EXP A TXP13C
EXP A TXN13	C1671	0.1U/4X7R/16V/K	EXP A TXN13C
EXP A TXP14	C1672	0.1U/4X7R/16V/K	EXP A TXP14C
EXP A TXN14	C1673	0.1U/4X7R/16V/K	EXP A TXN14C
EXP A TXP15	C1674	0.1U/4X7R/16V/K	EXP A TXP15C
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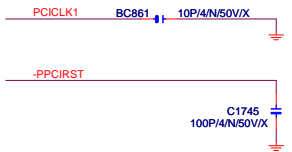
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Size Custom Document Number **GA-78LMT-S2PT** Rev **4.1**

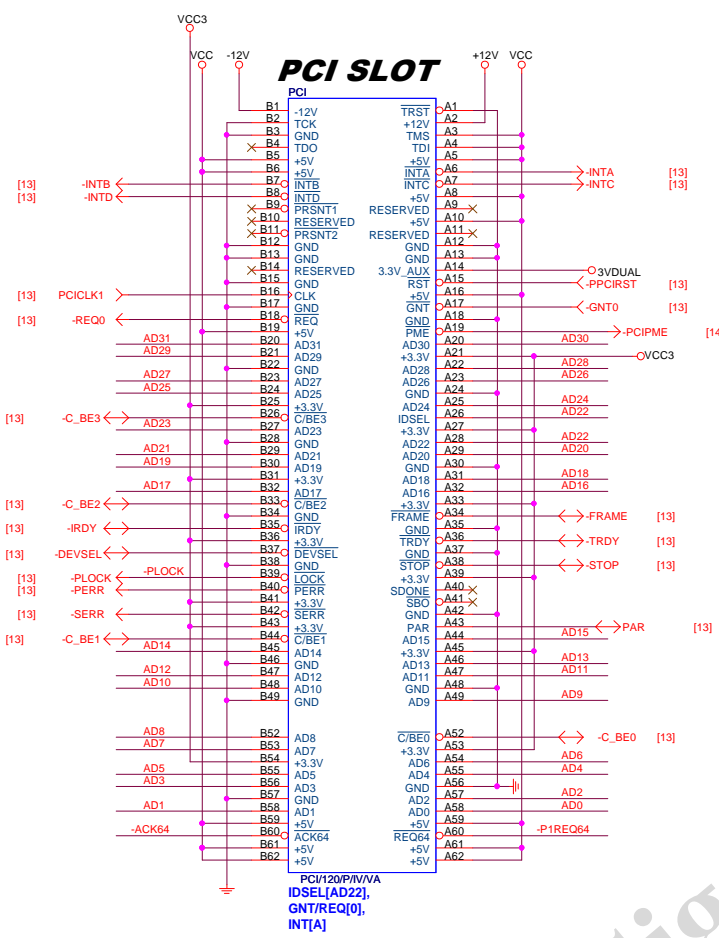
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PCI SLOT 1,2

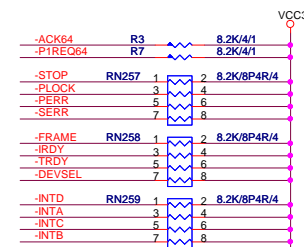
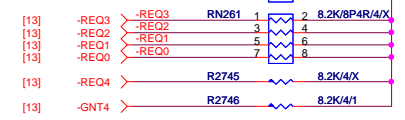
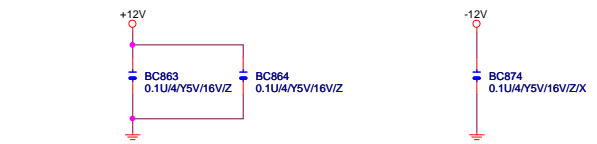
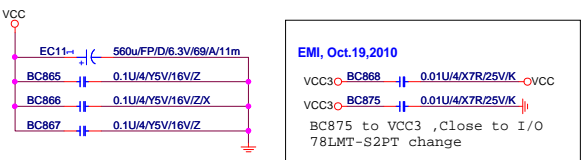
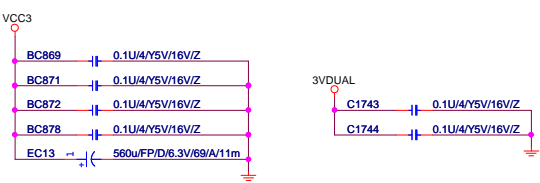
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PCI SLOT



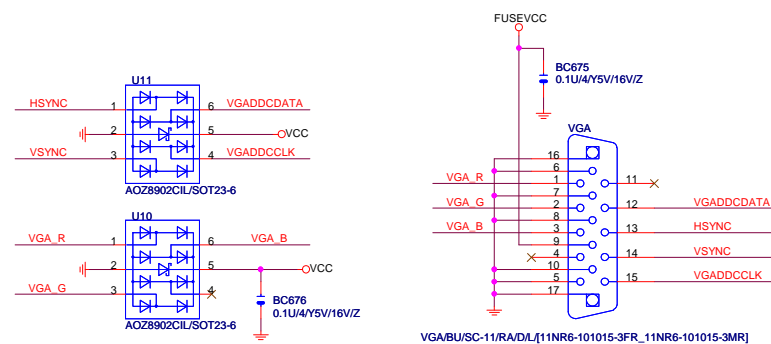
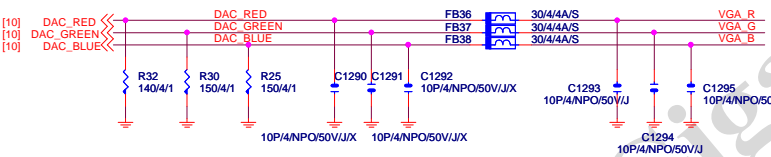
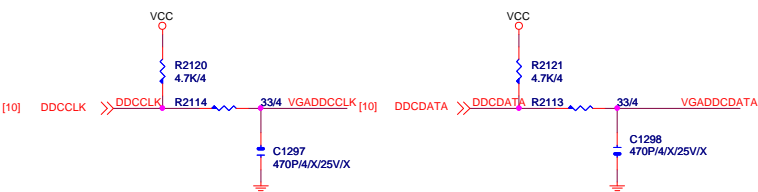
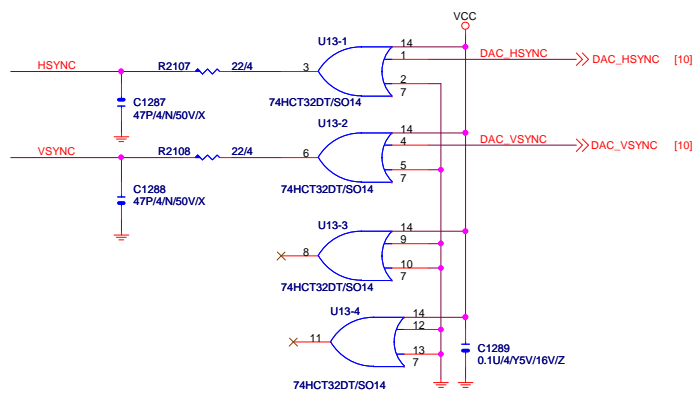
Gigabyte Confidential
Do not Copy



PCI SLOT 1,2

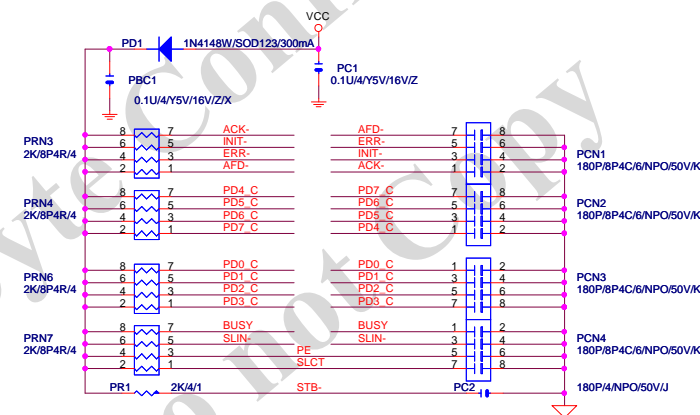
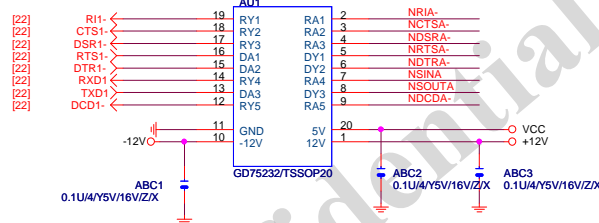
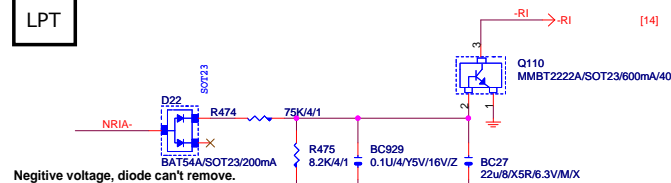
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VGA

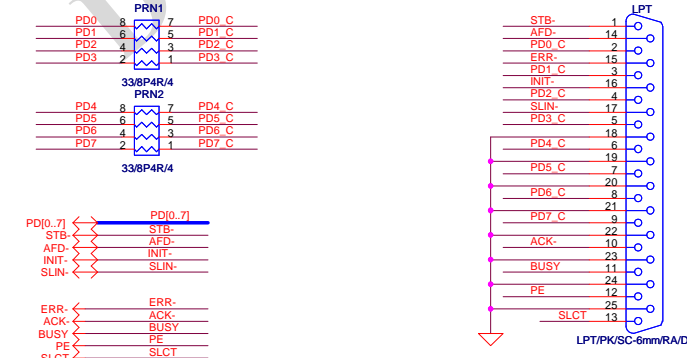


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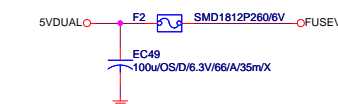
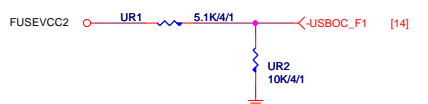
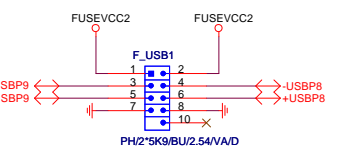
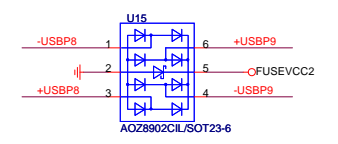
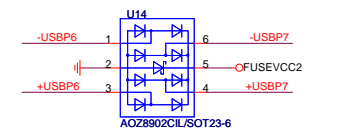
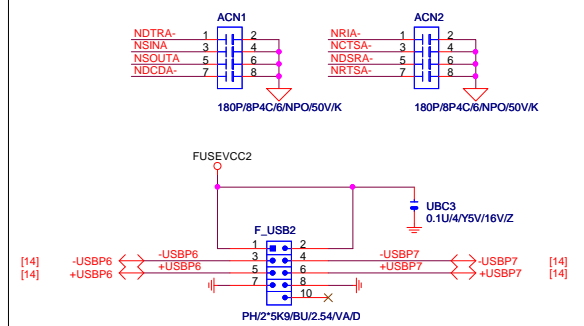
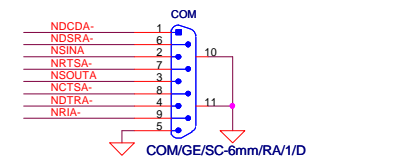
LPT



Fix Singel Glitch issue
,when put PCN1~4 Cap (ITE Recommend)



F_USB



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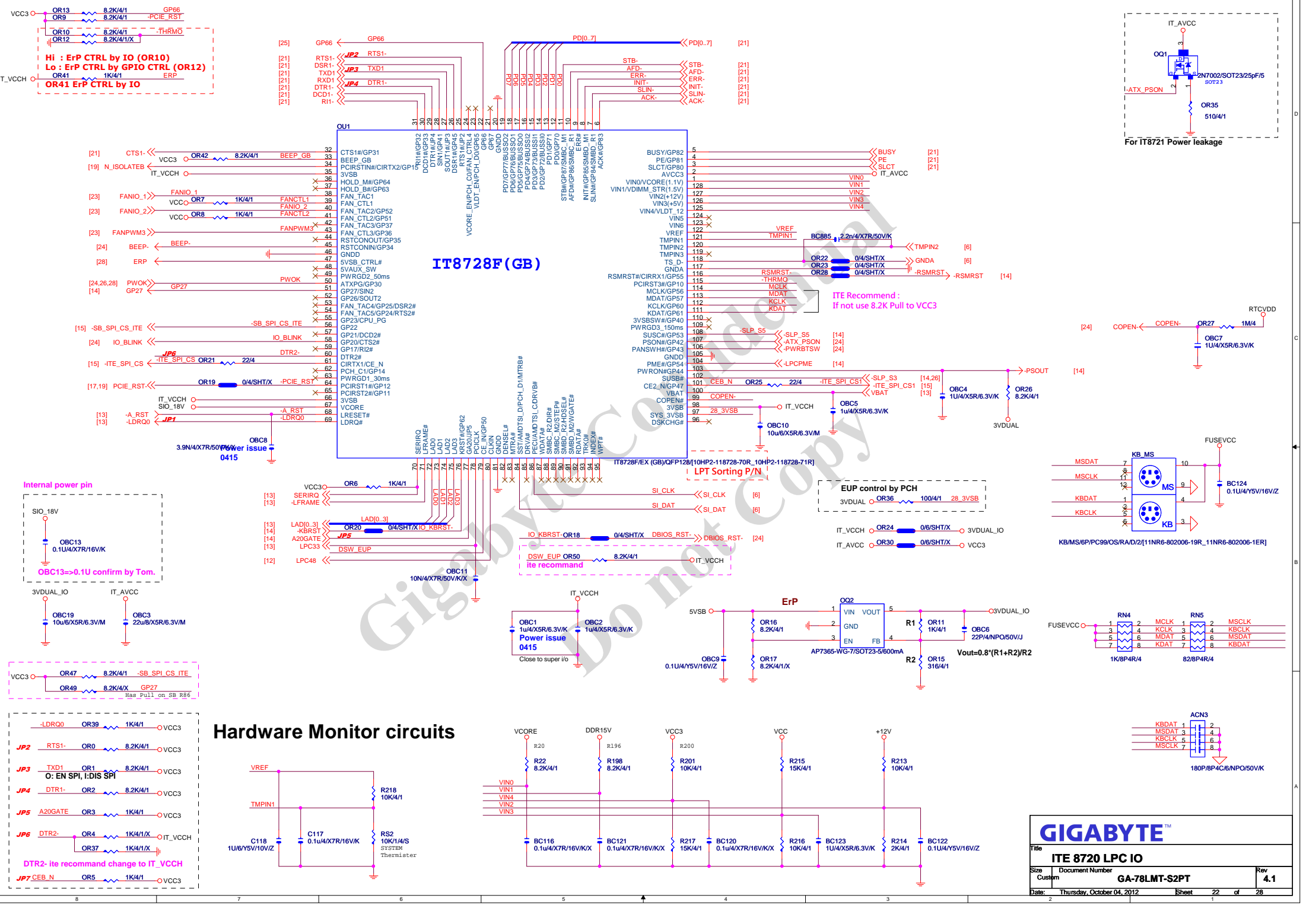
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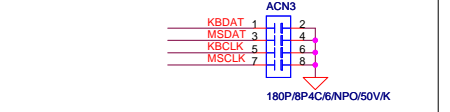
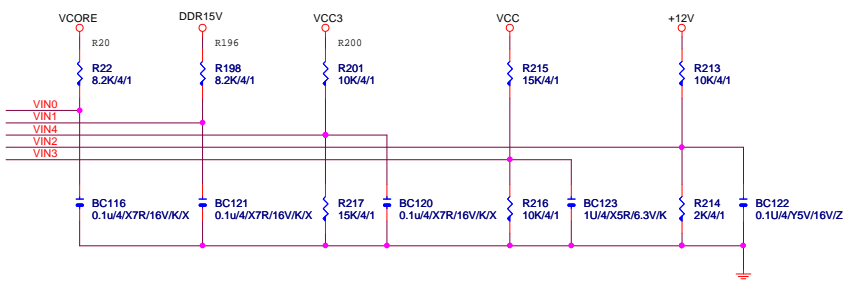
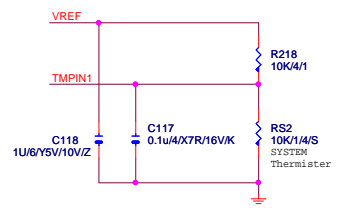
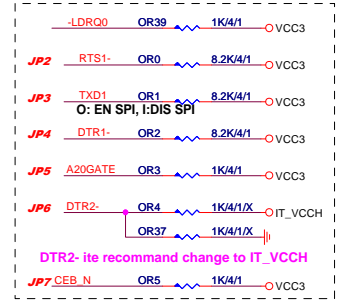
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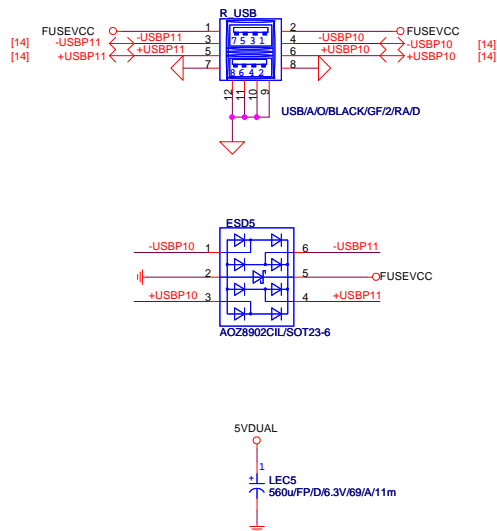
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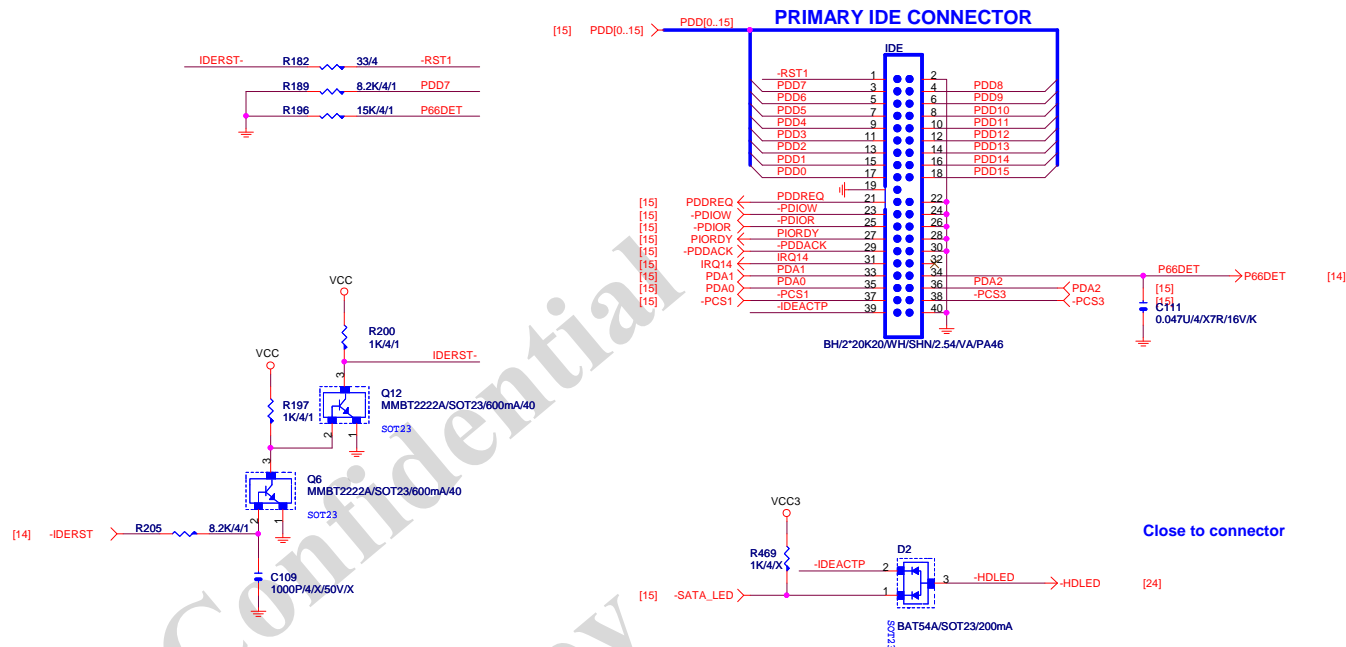
Hardware Monitor circuits



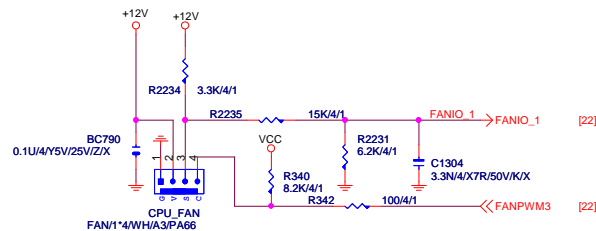
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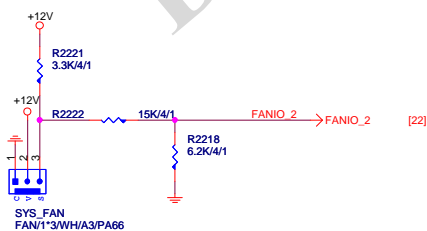
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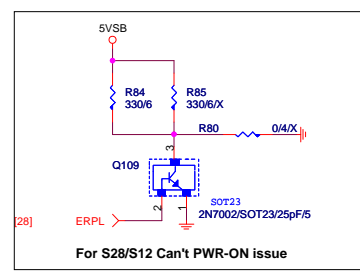
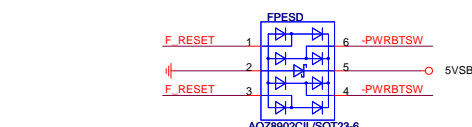
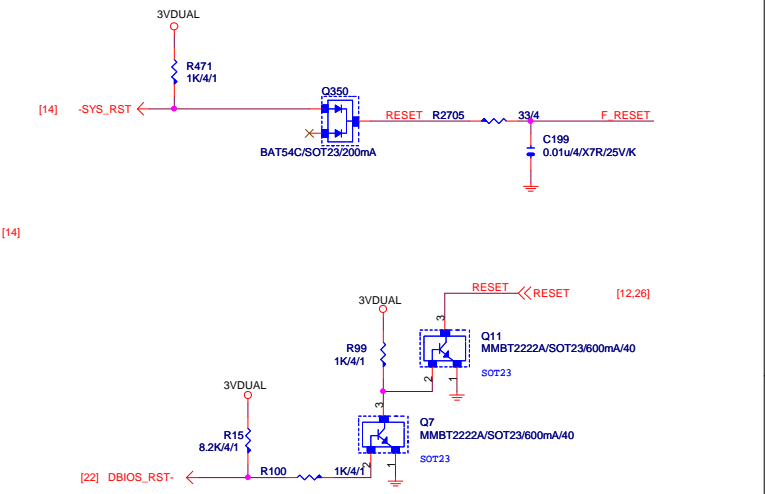
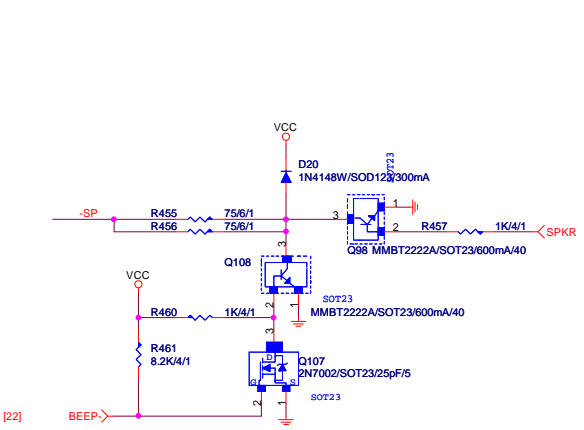
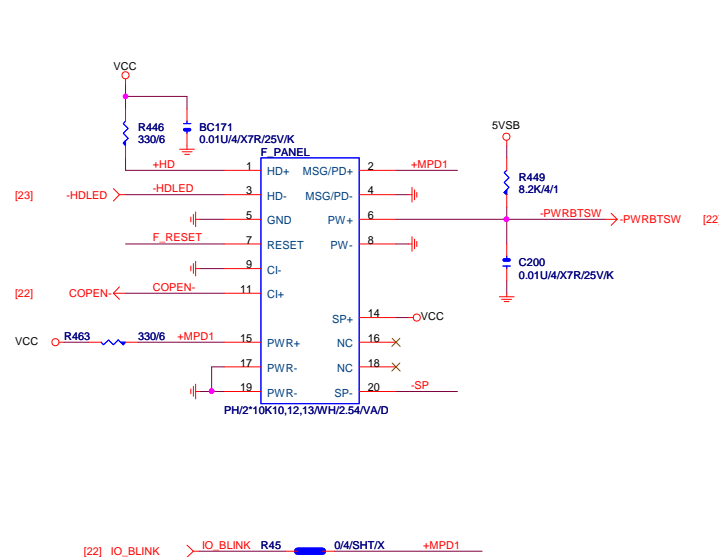


CPU_FAN

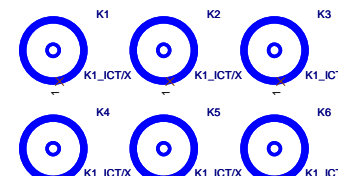
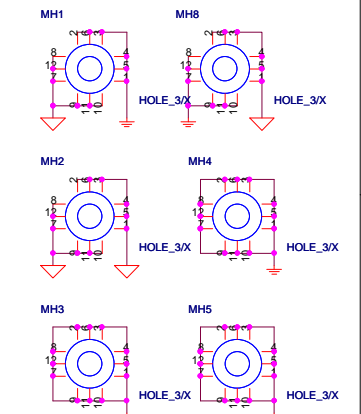
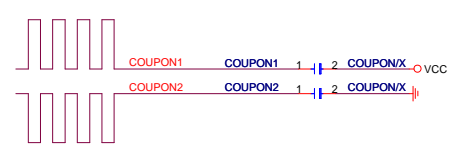
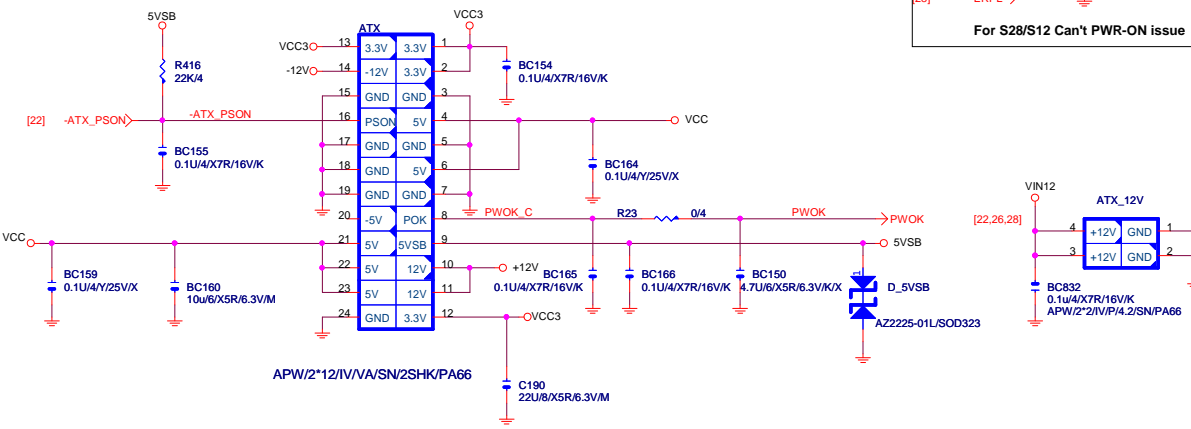


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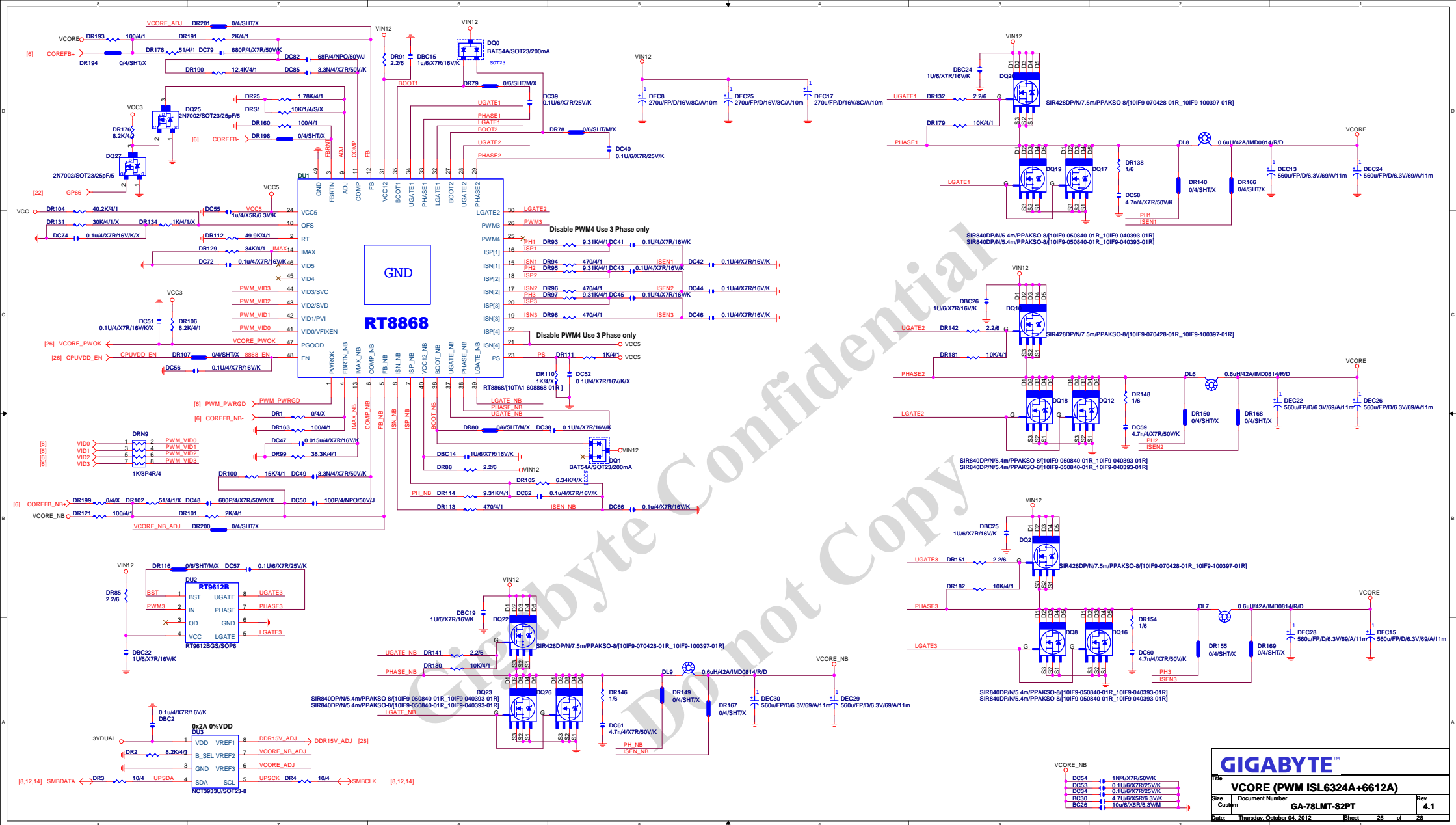


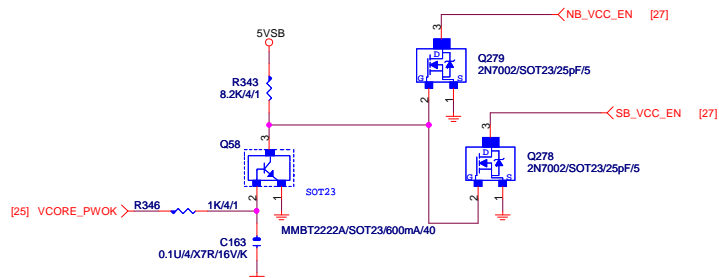
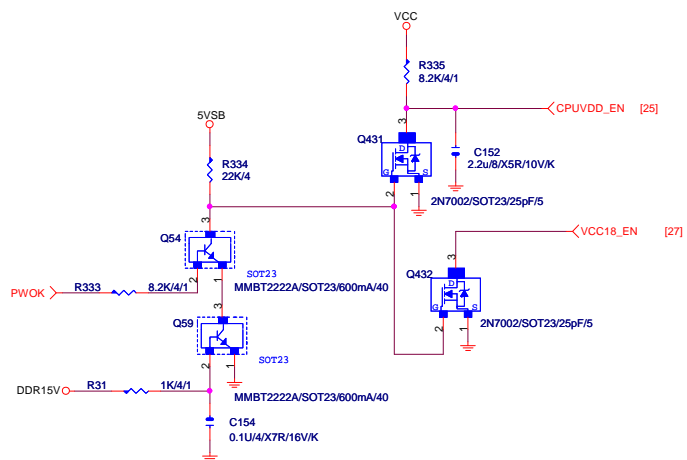
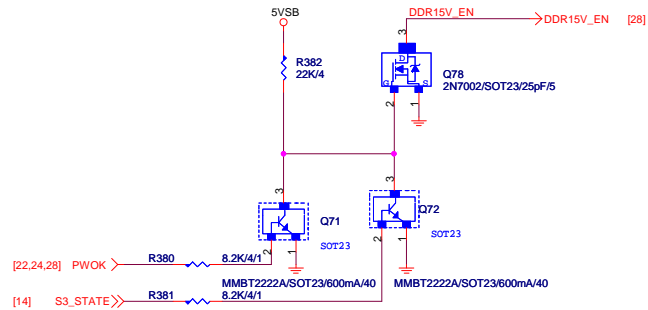


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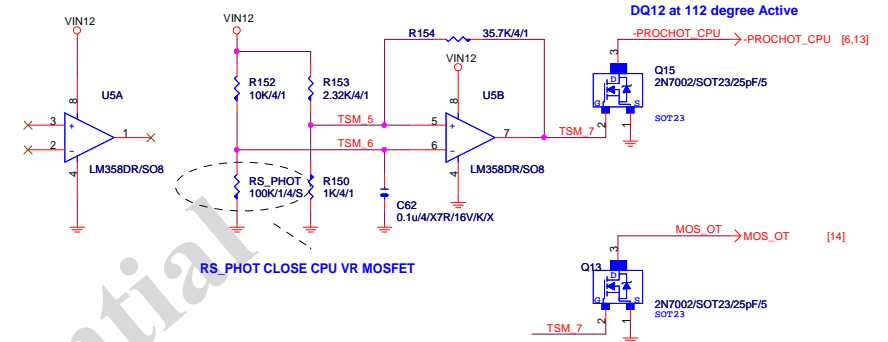


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Title ATX, FRONT PANEL			
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MOSFETHOT Protect

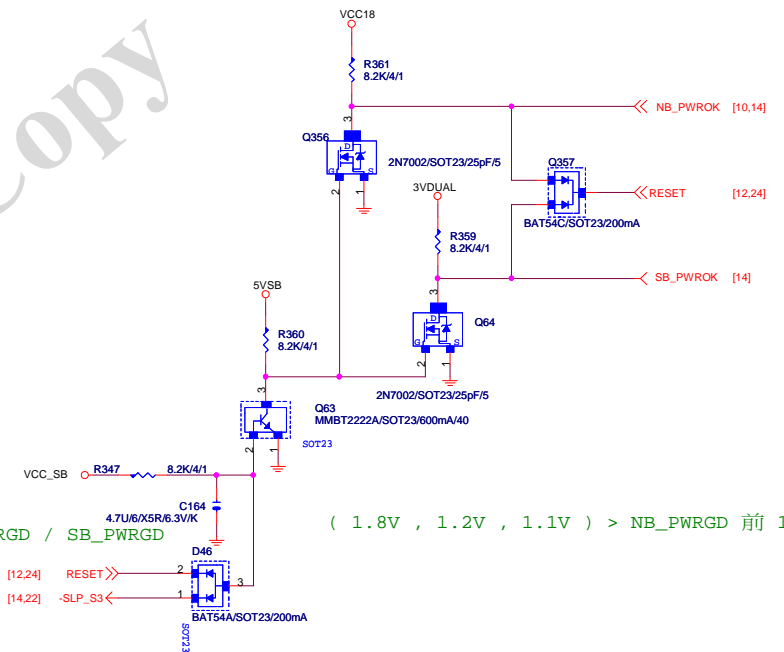


PWOK > NB_PWRGD / SB_PWRGD

[12,24] RESET

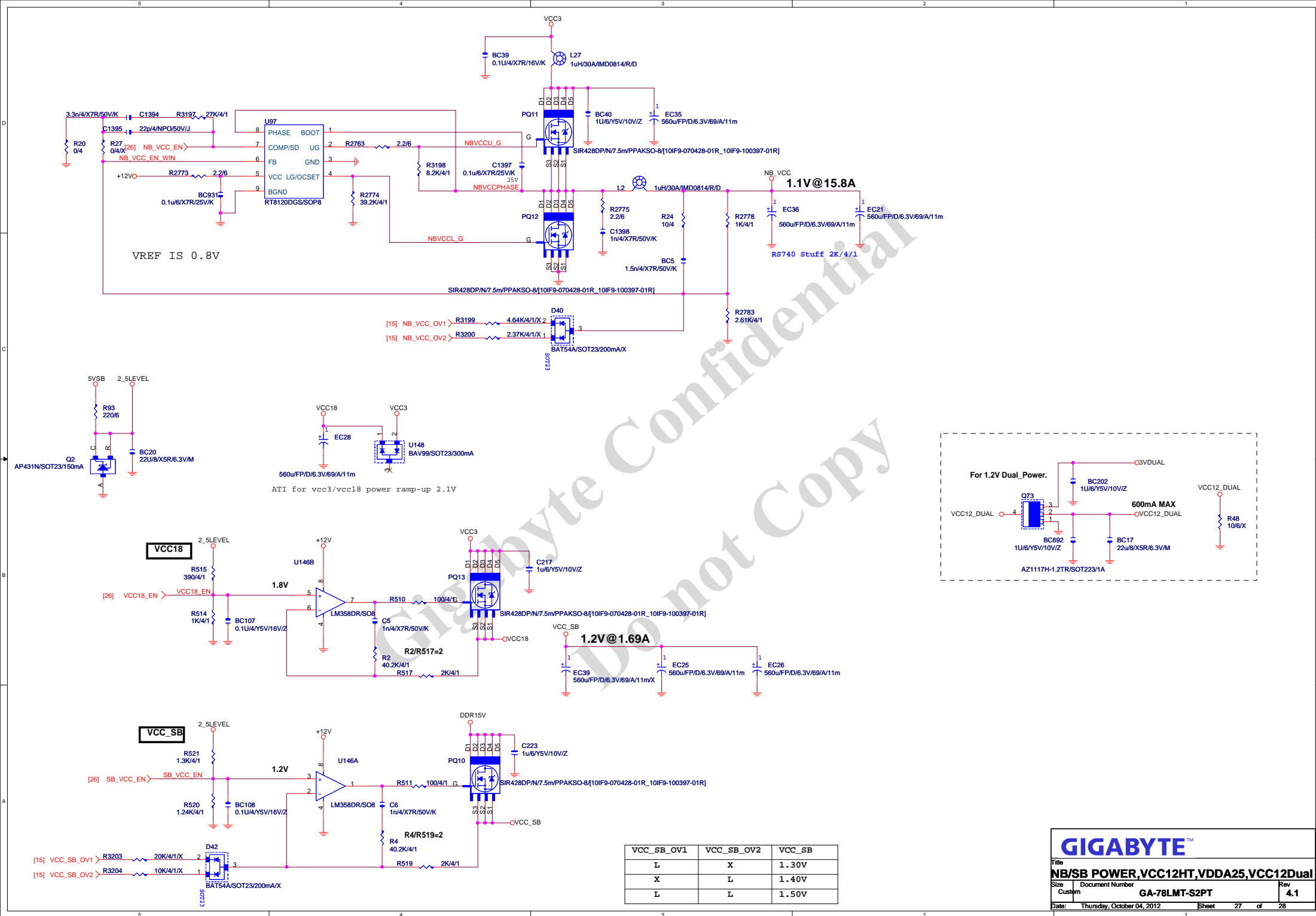
[14,22] -SLP_S3

(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms



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POWER SEQUENCE		
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VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V

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Title: NB/SB POWER, VCC12HT, VDDA25, VCC12Dual

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